SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

MK5025 TRANSPARENT MODE

INTRODUCTION

The SGS-Thomson X.25 Link Level Controller (MK5025) is a VLSI device which provides a complete link level data communication control conforming to the 1984 CCITT version of X.25. The MK5025 also supports X.32 (XID) and X.75 as well as single channel LAPD for ISDN with its UI frames and extended addressing capabilities.

One of the outstanding features of the MK5025 is its buffer managment which includes on-chip DMA. This feature allows users to handle multiple frames of receive and transmit data at a time. In order to utilize these buffer managment and DMA features with protocols not directly supported by the MK5025, a transparent mode is available for customized protocols using HDLC framing. This transparent mode provides an HDLC transport mechanism without link layer support. Extended addressing and control are optionally supported within transparent mode. Address filtering is also optional in this mode.

PURPOSE

The purpose of this application brief is to provide a detailed description of the MK5025 transparent mode and its options. Please refer to the MK5025 Technical Manual for more detailed information concerning the overall operation of the MK5025.

TRANSPARENT MODE ENTRY AND EXIT

To enter the transparent mode of operation, a user primitive *Trans* (UPRIM 3) is written to Control Status Register 1 (CSR1) after the completion of the first 4 steps of the *Initialization* procedure described in page 4-24 of the MK5025 Technical Manual. (The *Trans* Primitive is substituted for the *Start* primitive.) The transmitter then begins to output flags, and data frames are transmitted and received via the descriptor rings, but no protocol processing is done. Address and Control Fields are not prepended to the frames, and FCS (Frame Check Sequence) processing may be enabled or disabled by the DRFCS and DTFCS bits in the mode register, as described on page 4-12 of the Technical Manual. Transparent mode may be exited only with a *Stop* primitive (UPRIM 0) or by bus reset.

CONTROL AND STATUS REGISTER OPERATION

In transparent mode all the control and status register mechanisms are still functional, but there are several bits that pertain only to the protocols directly supported by the MK5025 and are not valid in transparent mode. The following is a list of the validity of the bits in each CSR and the mode register when in transparent mode.

CSR0 - All bits in this register are valid in Transparent mode. It should be noted that interrupts can only be set (by setting bit 09, INEA = 1) once the device is in start or transparent mode.

CSR1 - All bits except PPARM are valid, although only for a few non-protocol related conditions. Since in transparent mode only a Stop User Primitive would have been valid, User Primitives 8 and 9 have been redefined. When in transparent mode, issuing User Primitive 8 (UPRIM 8) will start T1 timer and User Primitive 9 (UPRIM 9) will stop it. In this case Provider Primitive 8 (PPRIM 8) has been redefined to indicate expiry of T1 timer.

CSR2 - Aside from the IADR bits, only the PROM and XIDE bits have valid meaning in transparent mode. The XIDE bit can be set to 1 to enable global address recognition, and the PROM bit is used to disable address filtering in transparent mode.

CSR3 - As in CSR2, the IADR bits contain the address of the first word in the Initialization Block. Bits 00 - 07 in CSR2 contain the high order 8 bits, and bits 00 - 15 of CSR3 contain the low order 16 bits of the address of the first word of the Initialization Block.

CSR4 - All bits in this register are valid in transparent mode, including the FIFO watermarks and bursting operations.

CSR5 - All bits are valid in transparent mode.

MODE REGISTER OPERATION

All bits in the Mode Register are valid including MFS (Minimum Frame Spacing) and LBACK (Loopback). However, bits 09 (EXTAF) and 10 (EXTCF) are useful mainly in transparent mode, for forcing extended address and control field filtering. The DACE bit also offers further flexibility in transparent mode by allowing address and con-

trol fields to be treated as normal data when DACE = 1, as shown in Table 2.

It should be noted that although DTFCS and DRFCS (bits 04 & 05) may be used to disable FCS generation and checking, the value in the FCS field of the received frame will not be stored in memory, even in transparent mode.

DESCRIPTOR RING OPERATION

The buffer management and descriptor ring operation is the same in transparent as non-transparent mode. It should be noted however that for the Transmit Message Descriptor, **TUI (bit 11 of TMD0) should be set to 1 for anything transmitted in transparent mode.** This is done because data transmitted in transparent mode is considered much the same as a UI frame rather than a normal I frame.

In transparent mode as in non-transparent mode, the Transmit Window size (TWD) in the Transmit Descriptor Ring Pointer must be set to a value greater than 0 for any transmission to occur. In fact, **if TWD=0 the MK5025 will not poll the Transmit Descriptor Ring.**

ADDRESS FIELD FILTERING AND CONTROL FIELD OPERATION

The frame structure for HDLC is as follows:

F	A	C	I	FCS	F

where:

F = Flag
A = Address field (A-field)
C = Control field (C-field)
FCS = Frame Check Sequence

According to HDLC rules, the A-field may be one or more octets in length. If the LSB of the first octet is 0, then the second octet is also part of the A-field. If the LSB of the second is 0, then the third octet is part of the A-field, and so on until an octet has an LSB = 1. The MK5025 allows the A-field to be one or two octets, depending upon the EXTA bit (Mode Register bit 10).

The C-field is one octet for modulo 8 for all frames. For modulo 128, the C-field is said to be extended, and is two octets for S (Supervisory) and I (Information) frames and one octet for U (Unnumbered) frames.

In the MK5025, address filtering and control field handling applies only to octet aligned frames received with good FCS. Any frame not meeting both of these conditions is discarded and the "Bad Frames Received" error counter (located at IADR + 44 of the Initialization Block) is incremented.

In the transparent mode, address filtering is supported if the PROM bit (CSR2, bit 10) is 0. In this case, frames are accepted if the received A-field matches either the Local Station Address or the Remote Station Address as specified in the Initialization Block. Bit RADR in the Receive Message Descriptor (RMD0 <09>)indicates which of the two programmable adresses the frame matched. This is a one octet compare if the extended address bit, EXTA is 0 (Mode register bit 06), or follows the HDLC rules for extended addressing if EXTA is 1. Frames not matching either address are ignored.

Extended control is also valid in transparent mode using the EXTC bit (Mode Register bit 07), as shown in Table 1 and Table 2. If EXTC is 0 then the C-field is one octet for all frames. If however EXTC is set to 1, the MK5025 will look to see if either of the two least significant bits of the C-field is 0. If so, the frame is said to have an extended control field which is two octets. In addition, bits EXTAF and EXTCF (Mode Register bit 09 & 10) are useful in transparent mode to force extended address and control. If EXTAF is set along with EXTA, the receiver will assume the ad-

Table 1: MK5025 Address Filtering Options

EXTA	EXTAF	XIDE	PROM	DACE	ADDRESS FILTERING
0	0	0	0	0	Single octet filtering L &R (Local & Remote adresses)
x	x	x	1	x	No address filtering, all frames accepted
0	0	1	0	0	Single octet filtering L & R and global
0	x	x	x	1	Not allowed
1	0	0	0	0	Double octet filtering L & R per HDLC rules
1	0	0	0	1	Double octet filtering L & R per HDLC rules
1	1	0	0	0	Double octet filtering L & R regardless of A-field LSB
0	1	x	x	0	Not allowed

Notes:
1) EXTA = Extended address, Mode register bit 06. EXTAF = Extended address Force, Mode register bit 09.

2) XIDE = XID enabled, CSR2 bit 08. PROM = Promiscuous mode, CSR2 bit 10.

3) DACE = Disable address and control field extraction for load to memory, Mode register bit 08.

4) L&R = Local and Remote addresses. X = Do not care.

Table 2: Address and Control Field Handling By the MK5025 Receiver

DACE	PROM	EXTA	EXTAF	EXTC	EXTCF	Address Field Handling	Control Field Handling
0	0	0	0	0	0	A filtered	CC ⇒ MEM1
0	0	0	0	1	0	A filtered	CC or EC ⇒ MEM1
0	0	1	0	0	0	A or EA filtered	CC ⇒ MEM1
0	0	1	1	0	0	EA filtered	CC ⇒ MEM1
0	0	1	0	1	0	A or EA filtered	CC or EC ⇒ MEM1
0	0	1	1	1	1	EA filtered	EC ⇒ MEM1
0	1	0	0	0	0	Not filtered, AA ⇒ MEM1	CC ⇒ MEM2
0	1	0	0	1	0	Not filtered, AA ⇒ MEM1	CC or EC ⇒ MEM2
0	1	1	0	0	0	Not filtered, AA or EA ⇒ MEM1	CC ⇒ MEM2
0	1	1	1	0	0	Not filtered, EA ⇒ MEM1	CC ⇒ MEM2
0	1	1	0	1	1	Not filtered, AA or EA ⇒ MEM1	EC ⇒ MEM2
1	0	X	X	X	X	First 2 octest always filtered	EC ⇒ MEM1
1	1	X	X	X	X	Total transparent mode	All data after opening flag & before FCS ⇒ memory

Notes:

1. MEM1 is the first location and MEM2 is the second location where received data is loaded. MEM1 and MEM2 are each 16 bits wide.

2. C is the received, single octet, control field. CC ⇒MEMx means the single octet control field C is loaded into both bytes of a 16 bit memory location. Similarly, A is a single octet address field, and AA ⇒ MEMx means the single octet address field A is loaded into both bytes of a 16 bit memory location.

3. EC is an extended control field (2 octets) for received S and I frames. For received U frames, the control field is not extended (1 octet). This determines whether CC or EC ⇒ MEMx. However, when EXTCF is set to 1, the control field is always extended (EC = 2 octets).

4. EA is an extended address field (2 octets). "A or EA filtered" means that one octet of the A-field is filtered if the LSB = 1, or two octets are filtered if the LSB = 0. Similarly "AA or EA ⇒ MEM1" means that AA is loaded into memory if the LSB = 0; else, EA is loaded. This conforms to HDLC rules for extended address. However, if EXTAF is set to 1, two octets are filtered regardless of the LSB, and EA will be loaded into memory.

5. EXTCF = Extended control force, Mode register bit 10.

6. DACE, PROM, EXTA, EXTAF, and EXTC are as defined in the notes for Table 1. X = Do not care.

dress field to be two bytes long regardless of the first bit of the address field. If EXTCF is set along with EXTC, the receiver will assume the contol field to be two bytes long regardless of the first two bits of that field.

For global adresses, the XIDE bit is valid in transparent mode, depending upon the settings of the other bits in the Mode Register, as shown in Table 1. If XID is enabled by setting bit XIDE (CSR2 bit 08) to 1, then all frames with address "11111111" are accepted. Even frames which are not XID are accepted. In this case, a global address is considered as a command frame. Additionally, frames may transmitted from the XID/TEST buffer, but neither an Address nor Control field will be pre-pended to the frame.

Address and control field extraction can be disabled in transparent mode, through use of the if PROM bit (CSR2, bit 10) and DACE bit (Mode Register bit 08), as shown in Table 2. If the PROM bit is 1, all frames are accepted. When both the PROM bit and the DACE bit are set to 1, the device is considered to be in total transparent mode. In this mode no protocol processing is done and all data after the opening flag and before the FCS is loaded into memory.

CONCLUSION

The MK5025 offers great flexibility to the data communications system designer. The on-chip protocol processing may be used to save the designer much time in implementing standard protocols such as X.25, LAPB, ISDN LAPD, X.32, and X.75, while still allowing the flexibility of implementing alternate or customized HDLC based protocols using the MK5025's transparent mode.